09/834297

COFC

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): David R. Hembree

Patent No.: 6,806,567 B2

Issued: October 19, 2004

For: CHIP ON BOARD WITH HEAT SINK ATTACHMENT AND ASSEMBLY

Attorney Docket No.: 2269-3592.5US

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

March 13, 2007 Leta M. Howard
Date Signature

Leta M. Howard
Name (Type/Print)

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT OFFICE MISTAKES (37 C.F.R. § 1.322)

Attn.: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

It is noted that several errors appear in this patent of a typographical nature. These errors are due to mistakes in printing on the part of the U.S. Patent and Trademark Office, and occurred through no fault of the Applicant. A certificate of correction in the form attached hereto is requested.

Please note that an Amendment Pursuant to 37 C.F.R. § 1.312(a) (copy enclosed) was filed concurrently with the issue fee on December 22, 2003. Attached is a copy of the previously-filed Amendment Pursuant to 37 C.F.R. § 1.312(a) and the date-stamped postcard, acknowledging receipt by the PTO, to provide proof of such filing. The PTO inadvertently printed the annotated sheets of the drawing amendments on the printed patent instead of the replacement sheets included with the Amendment Pursuant to 37 C.F.R. § 1.312(a). We have

included subject matter of this amendment on the attached PTO/SB/44 with at least one copy being suitable for printing.

Please send the Certificate to:

Name: James R. Duzan
Address: TraskBritt
P.O. Box 2550
Salt Lake City, Utah 84110

Attached hereto in duplicate is Form PTO/SB/44 with at least one copy being suitable for printing.

Respectfully submitted,

James R. Duzan

James R. Duzan
Registration No. 28,393
Attorney for Applicant(s)
TRASKBRITT
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Telephone: 801-532-1922

Date: March 13, 2007
JRD/csw

Enclosures: PTO/SB/44 in duplicate
Copy of Amendment Pursuant to 37 C.F.R. § 1.312(a)
Copy of date-stamped postcard
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PTO/SB/44 (04-04)
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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 6,806,567 B2
DATED : October 19, 2004
INVENTOR(S) : David R. Hembree

It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the specification:

COLUMN 6, LINE 38, change "elastomer **50**" to --elastomer **150**--

In the drawings:

FIGURE 3A,	delete the lower lead line of "32" (right-most occurrence) (already crossed out)
FIGURE 3D,	shorten the lead line of "44" to better indicate the exposed surface (excess already crossed out)
FIGURE 3G,	shorten the lead line of "44" to better indicate the exposed surface (excess already crossed out), shorten the lead line of "22" to better indicate the wire (excess already crossed out), and add the reference numeral --18--with appropriate lead line (already handwritten in)
FIGURE 4A,	delete the lower lead line of "32" (right-most occurrence) (already crossed out)
FIGURE 4E,	change "3" to --38-- (both occurrences) (already crossed out and handwritten in)
FIGURE 5,	shorten the lead line of "14" to better indicate the active surface (excess already crossed out)

MAILING ADDRESS OF SENDER:

PATENT NO. 6,806,567 B2

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UNITED STATES PATENT AND TRADEMARK OFFICE

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INVENTOR(S) : David R. Hembree

It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

In the drawings (continued):

FIGURE 7, shorten the lead line of "14" to better indicate the active surface (excess already crossed out), and delete reference numeral "64" with corresponding lead line (already crossed out)

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INVENTOR(S) : David R. Hembree

It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Replace FIG. 3A with the following:

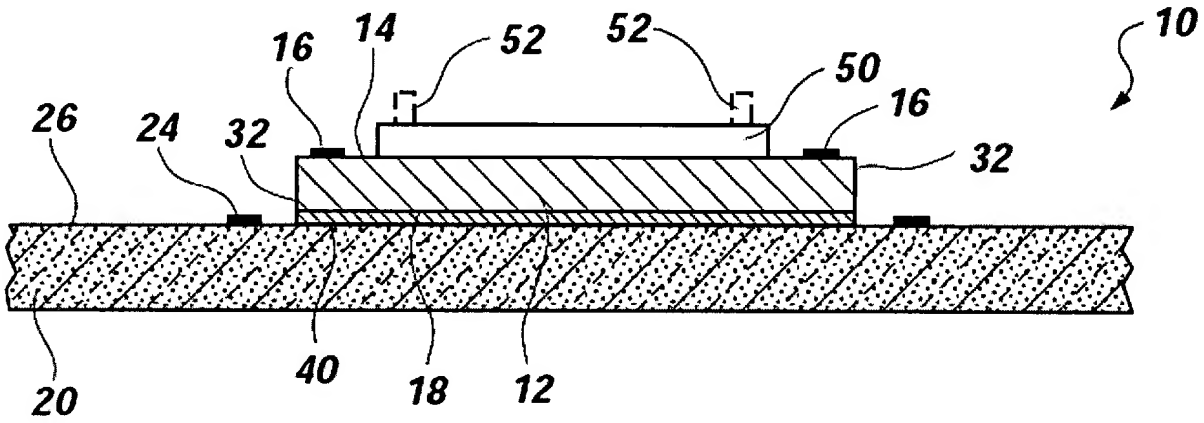

Fig. 3A

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It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Replace FIG. 3D with the following:

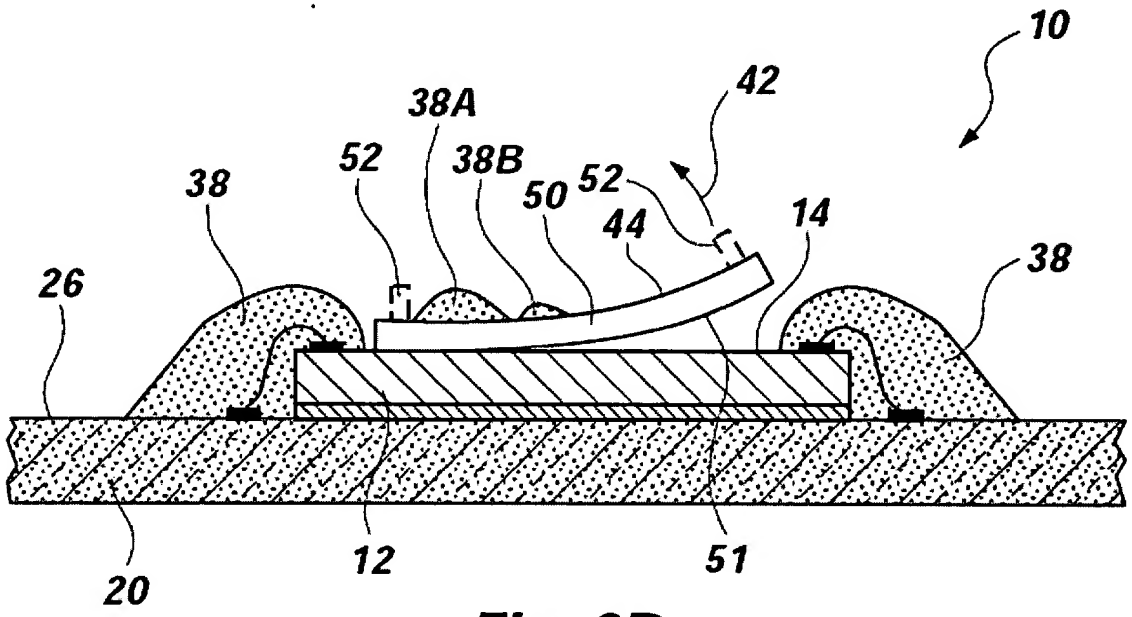

Fig. 3D

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It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Replace FIG. 3G with the following:

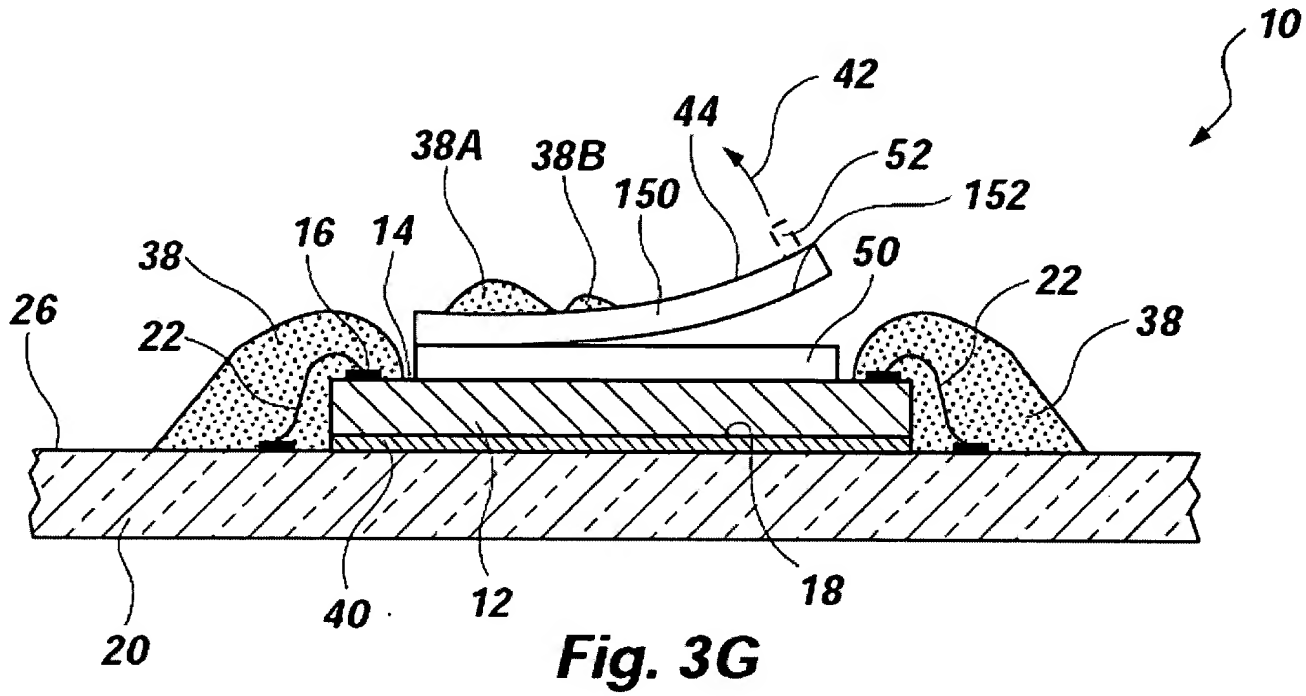

Fig. 3G

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DATED : October 19, 2004
INVENTOR(S) : David R. Hembree

It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Replace FIG. 4A with the following:

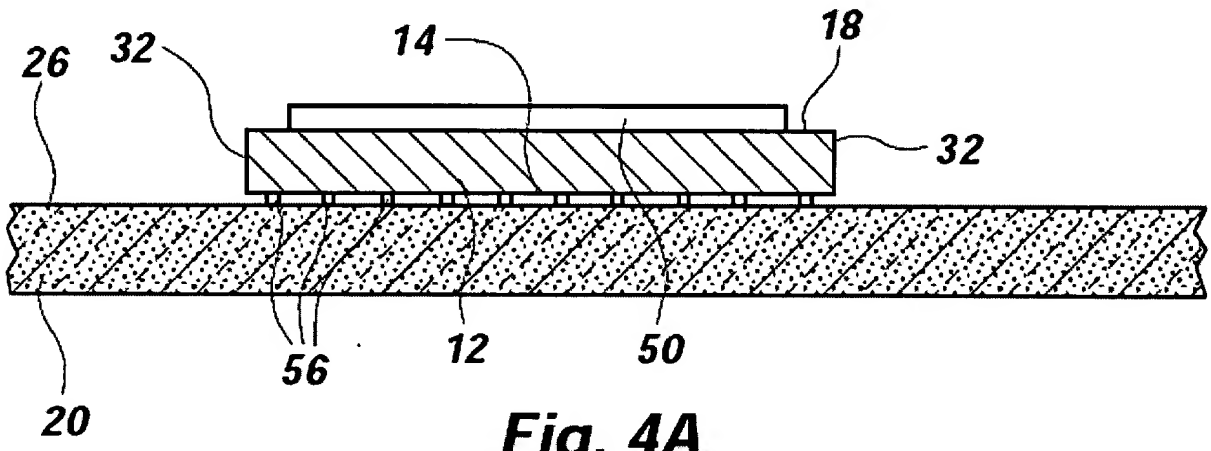

Fig. 4A

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INVENTOR(S) : David R. Hembree

It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Replace FIG. 4E with the following:

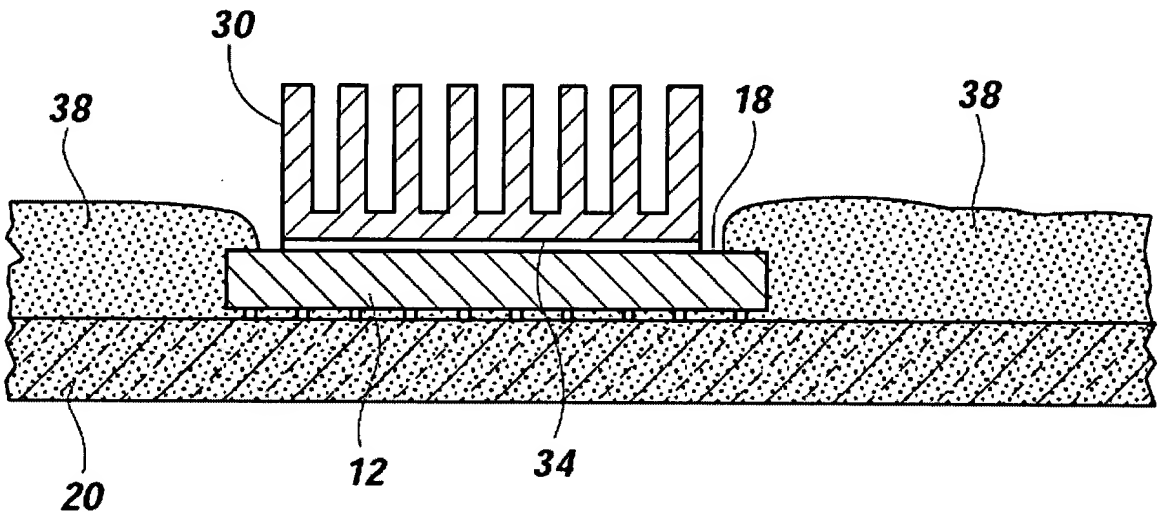

Fig. 4E

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PATENT NO : 6,806,567 B2
DATED : October 19, 2004
INVENTOR(S) : David R. Hembree

It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Replace FIG. 5 with the following:

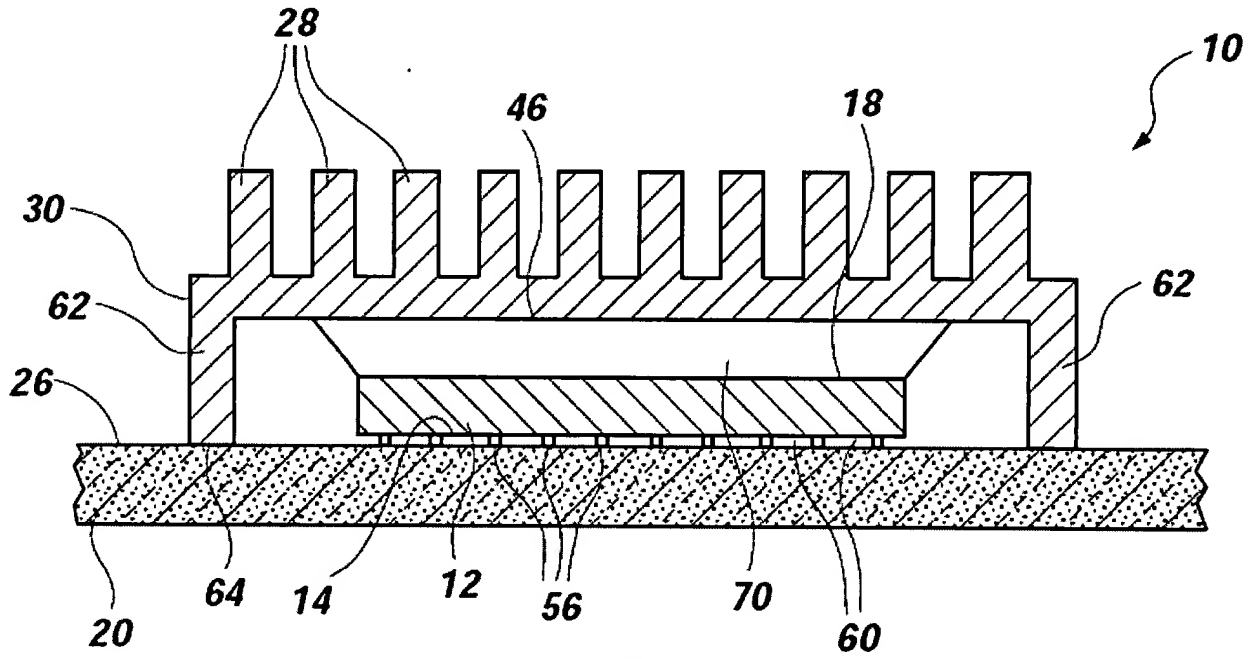

Fig. 5

MAILING ADDRESS OF SENDER:

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INVENTOR(S) : David R. Hembree

It is certified that errors appear in the above-identified patent and that said Letters Patent are hereby corrected as shown below:

Replace FIG. 7 with the following:

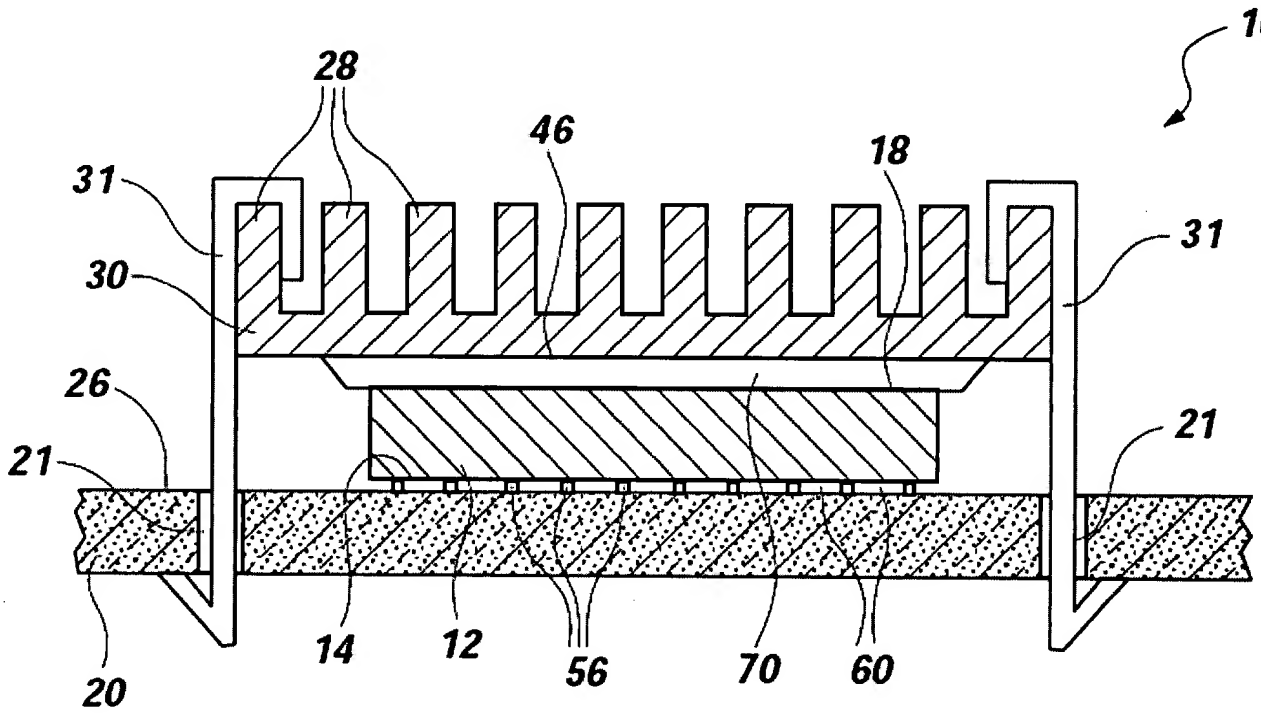

Fig. 7

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TH[illegible]TENT & TRADEMARK OFFICE MAILROOM[illegible]E
STAMPED HEREON IS AN ACKNOWLEDGEMENT THAT ON THIS DATE THE PATENT & TRADEMARK OFFICE RECEIVED:

Transmittal Letter (2 pages, w/duplicate copy); Part B - Fee(s) Transmittal (1 page w/duplicate copy); Check No. 19728 in the amount of $1645.00; Amendment Pursuant to 37 C.F.R. § 1.312(a) (8 pages); and Fee Addressee for Receipt of PTO Notices Relating to Maintenance Fees (2 pages).

Invention:	CHIP ON BOARD WITH HEAT SINK ATTACHMENT
Applicant(s):	David R. Hembree
Filing Date:	April 12, 2001
Serial No.:	09/834,297
Date Sent:	December 22, 2003 via first class mail
Docket No.:	2269-3592.5US
JRD/sls:djp	

MAR 2 0 2007

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

David R. Hembree

Serial No.: 09/834,297

Filed: April 12, 2001

For: CHIP ON BOARD WITH HEAT SINK ATTACHMENT

Confirmation No.: 6489

Examiner: J. Mitchell

Group Art Unit: 2827

Attorney Docket No.: 2269-3592.5US
(97-0321.05/US)

Notice of Allowance Mailed:

September 23, 2003

CERTIFICATE OF MAILING

I hereby certify that this correspondence along with any attachments referred to or identified as being attached or enclosed is being deposited with the United States Postal Service as First Class Mail on the date of deposit shown below with sufficient postage and in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

December 22, 2003
Date

Signature

Deidra J. Pfeil
Name (Type/Print)

AMENDMENT PURSUANT TO 37 C.F.R. § 1.312(a)

Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

Please amend the above-referenced application as follows:

Amendments to the Title appear on page 3 of this paper.

Amendments to the Specification appear on page 4 of this paper.

Amendments to the Claims are reflected in the listing of claims which begins on page 5 of this paper.

Amendments to the Drawings appear on page 7 of this paper and include both attached replacement sheets and annotated sheets showing changes.

Remarks begin on page 8 of this paper.

An **Appendix A** including a clean version of the amended substitute specification is attached following page 8 of this paper.

An **Appendix B** including a marked-up version of the amended substitute specification showing changes made is attached following Appendix A of this paper.

An **Appendix A** including amended drawing figures is attached following Appendix B of this paper.

IN THE TITLE:

The title has been amended herein. Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date), please enter the title as amended.

CHIP ON BOARD WITH HEAT SINK ATTACHMENT AND ASSEMBLY

IN THE SPECIFICATION:

Pursuant to 37 C.F.R. §§ 1.121 and 1.125 (as amended to date) please enter the substitute specification in clean form and including paragraph numbers **[0001]** through **[0065]** and Abstract attached hereto as Appendix A. A marked-up substitute specification to clearly identify amendments to the specification as required by 37 C.F.R. § 1.121(b)(3)(iii) is attached hereto as Appendix B. It is respectfully submitted that the substitute specification does not introduce new matter into the above-referenced patent application.

IN THE CLAIMS:

Claims 3-5, 8 and 9 were previously cancelled. Claim 6 has been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Listing of Claims:

1. (Previously presented) A semiconductor assembly comprising:

a substrate having a surface;

a semiconductor die having a plurality of edges, having an active surface having a plurality of bond pads thereon located adjacent at least two edges of the plurality of edges, and having a back side surface, the semiconductor die having at least a portion of the back side surface adhesively attached to at least a portion of the surface of the substrate;

a gel elastomer contacting at least a portion of the active surface of the semiconductor die;

a layer of adhesive substantially covering a surface of the gel elastomer;

a heat sink attached to the gel elastomer by the layer of adhesive; and

an encapsulation material covering a portion of the surface of the substrate, the plurality of edges of the semiconductor die, and at least one bond pad of the plurality of bond pads located adjacent at least two edges of the semiconductor die, wherein the encapsulation material excludes covering the heat sink.

2. (Original) The semiconductor assembly of claim 1, wherein the heat sink includes a plurality of fins thereon.

3.-5. (Cancelled)

6. (Currently amended) A semiconductor assembly comprising:

a substrate having a plurality of electrical connections on a portion of a surface thereof;

at least one semiconductor die having a plurality of bond pads on a first portion of an active surface thereof and having a back side surface, a portion of the back side surface adhesively attached to a portion of the surface of the substrate;

a plurality of wire bonds connecting at least a portion of the plurality of bond pads of the at least one semiconductor die to at least a portion of the plurality of electrical connections of the ~~substrate~~ substrate, a gel elastomer contacting a second portion of the active surface of the at least one semiconductor die;

a layer of adhesive substantially covering a surface of the gel ~~elastomer~~ elastomer;

a heat sink attached to the gel elastomer by the layer of adhesive; and

an encapsulant material covering a portion of the surface of the substrate, the plurality of bond pads on the active surface of the at least one semiconductor die, a portion of the active surface of the at least one semiconductor die, and the plurality of wire bonds, wherein the encapsulation material excludes covering the heat sink.

7. (Original) The semiconductor assembly of claim 6, wherein the heat sink includes a plurality of fins thereon.

8. (Cancelled)

9. (Cancelled)

IN THE DRAWINGS:

The attached sheets of drawings include changes to FIGS. 3A, 3D, 3G, 4A, 4E, 5 and 7. These sheets, which include FIGS. 3A-3D, 3E-3G, 4A-4D, 4E-4F, and 5-7, replace the original sheets including FIGS. 3A-3D, 3E-3G, 4A-4D, 4E-4F, and 5-7.

Specifically, FIG. 3A has been revised to delete the lowest lead line extending from reference numeral "32" in the right-hand portion of the figure; FIG. 3D has been revised to shorten the lead line extending from reference numeral "44" to better indicate the exposed surface; FIG. 3G has been revised to shorten the lead line extending from reference numeral "44" to better indicate the exposed surface, to shorten the lead line extending from reference numeral "22" in the left-hand portion of the figure to better indicate the wire, and to add the reference numeral --18-- with appropriate lead line; FIG. 4A has been revised to delete the lowest lead line extending from reference numeral "32" in the right-hand portion of the figure; FIG. 4E has been revised to change the reference numeral "3" (two occurrences) to --38--; FIG. 5 has been revised to shorten the lead line extending from reference numeral "14" to better indicate the active surface; and FIG. 7 has been revised to shorten the lead line extending from reference numeral "14" to better indicate the active surface and to delete reference numeral "64" with corresponding lead line. No new matter has been added.

REMARKS

This amendment corrects errors in the text and drawings. Entry is respectfully solicited.

This amendment is submitted prior to or concurrently with the payment of the issue fee and, therefore, no petition or fee is required. No new matter has been added.

Respectfully submitted,

James R. Duzan

James R. Duzan
Registration No. 28,393
Attorney for Applicant(s)
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

Date: December 22, 2003
JRD/csw

Enclosures: Appendices A and B
Replacement Sheets
Annotated Sheets Showing Changes

\\Traskbritt1\Shared\DOCS\2269-3592.5US\56153.doc

APPENDIX A

(CLEAN VERSION OF SUBSTITUTE SPECIFICATION)

(Serial No. 09/834,297)

PATENT
Attorney Docket 3592.5US (97-321.5)

NOTICE OF EXPRESS MAILING

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APPLICATION FOR LETTERS PATENT

for

CHIP ON BOARD WITH HEAT SINK ATTACHMENT AND ASSEMBLY

Inventor:
David R. Hembree

Attorney:
James R. Duzan
Registration No. 28,393
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
(801) 532-1922

MAR 20 2007

CHIP ON BOARD WITH HEAT SINK ATTACHMENT AND ASSEMBLY

BACKGROUND OF THE INVENTION

[0001] Cross-Reference to Related Applications: This application is a continuation of application Serial No. 09/510,894, filed February 23, 2000, now U.S. Patent 6,229,204 B1, issued May 8, 2001, which is a divisional of application Serial No. 09/146,945, filed September 3, 1998, now U.S. Patent 6,117,797, issued September 12, 2000.

[0002] Field of the Invention: This invention relates generally to integrated circuit packages and methods of package assembly. More particularly, the present invention pertains to the manufacture of Chip On Board devices with heat sinks for high power dissipation.

[0003] State of the Art: Semiconductor devices are used in a wide variety of products, including computers, automobiles, integrated circuit cards, audio/video products, and a plethora of other electronic apparatus.

[0004] Modern electronic appliances such as computers have hundreds of integrated circuits (IC) and other electronic components, most of which are mounted on printed circuit boards (PCB). Heat is generated by such components. The heat generated by many ICs and other electronic components with simple circuits may often be dissipated without an additional heat sink. However, components requiring added heat sinks are becoming more numerous as the required speed, circuit complexity, and circuit density have increased.

[0005] In particular, as semiconductor devices have become more dense in terms of electrical power consumption per unit volume, heat generation has greatly increased, requiring package construction which dissipates the generated heat much more rapidly. As the state of the art progresses, the ability to adequately dissipate heat is often a severe constraint on the size, speed, and power consumption of an integrated circuit design.

[0006] The term "heat sink" is used herein in general reference to a passive heat transfer device, for example, an extruded aluminum plate with or without fins thereon. The plate is thermally coupled to an electronic component, e.g., semiconductor die, to absorb heat from the component and dissipate the heat by convection into the air. In this application, a heat sink will be distinguished from a "heat spreader," the latter pertaining to a member which channels heat

from a semiconductor die to leads which exit the die package. However, a heat sink and a heat spreader may together be used to cool a device.

[0007] Integrated circuit devices are constructed by making, e.g., a (silicon or germanium) semiconductor die with internal and surface circuits including transistors, resistors, capacitors, etc. A single semiconductor die may contain thousands of such components and generate considerable heat. Electrical connection pads on an "active" surface of the semiconductor die are connected to the various die circuits. The integrated circuit device also includes electrical leads enabling the electrical connection pads of the semiconductor die to be connected to circuits on a PCB (or other substrate) of an appliance.

[0008] Dissipation of generated thermal energy is necessary for safe operation of an electronic appliance. An excessively high temperature of an IC may cause a circuit board fire and damage or destroy the appliance. High temperatures cause failure of the integrated circuits themselves. State of the art methods for absorbing and dissipating thermal energy from high speed Chip On Board (COB) semiconductor devices are inadequate for any or all of the following reasons: (a) insufficient heat transfer capability, (b) excessively large package size, especially the profile height, (c) complexity of manufacture, and/or (d) excessive cost.

[0009] Current methods of forming glob topped Chip On Board devices with heat sinks are shown in United States Patent 5,552,635 of Kim et al., United States Patent 5,477,082 of Buckley III et al., United States Patent 5,468,995 of Higgins III, United States Patent 5,610,442 of Schneider et al., and United States Patent 5,659,952 of Kovac et al.

[0010] In United States Patent 5,450,283 of Lin et al., a method for making a semiconductor device with an exposed die back side is described. The method includes providing a printed wiring board (PWB) substrate with conductive traces, on which a semiconductor die is flip mounted and connected to the conductive traces. An electrically nonconductive coupling material is placed between the die and substrate. A package body is formed around the perimeter of the die, covering a portion of the conductive traces and any portion of the coupling material extending beyond the die perimeter. The back side of the die is left exposed through the use of a thin layer of tape placed in the mold cavity prior to the transfer molding of the package body around the die to prevent the flow of molding material forming the

package from flowing on the inactive back side of the die. If the thin layer of tape adheres to the die after removal of the semiconductor device from the mold cavity, the thin layer of tape is removed from the die of the semiconductor device.

[0011] A device made with multiple layers of encapsulant is shown in United States Patent 5,379,186 of Gold et al.

SUMMARY OF THE INVENTION

[0012] In accordance with the invention, an improved method for fabricating a Chip On Board semiconductor device requiring enhanced heat dissipation is applicable to direct attachment of semiconductor devices, such as dynamic memory semiconductor dice, to substrates, such as circuit boards and the like, and to the formation of modules incorporating a substrate, such as a circuit board.

[0013] In one aspect of the invention, an elastomer is used to cover a portion of a semiconductor die prior to glob top application of the die to the circuit board. The elastomer is removed, e.g., by peeling, from the die surface and includes any glob top material which has inadvertently been applied to the elastomer. Thus, the portion of the semiconductor die remains free of contaminants. If desired, since a portion of the semiconductor die is free of contaminants, providing a good adhesion surface, a heat sink may be attached to such portion of the semiconductor die. The method is applicable to both wire-bonded dice and flip-chip die bonding to circuit boards. Alternatively, the elastomer may be retained on a portion of the semiconductor die after the molding or glob-topping of the die for the attachment of a heat sink thereto, if desired. The elastomer may be a highly thermally conductive elastomer to enhance the heat transfer from the semiconductor die to the surrounding environment. An example of a highly thermally conductive elastomer is a metal-filled elastomer or an elastomer filled with a highly thermally conductive material like metal.

[0014] The preferred elastomer is highly heat conductive, very compliant, has a relatively low adhesiveness and a high surface wetting property, all the type of properties that enhances heat transfer from the semiconductor die.

[0015] In another aspect of the invention, a heat conductive cap is formed over a semiconductor die and comprises a heat sink. A layer of the metal filled gel elastomer is placed between the non-active surface of a die and the cap. Compressing the die into the cap forms the desired adhesion to retain the die within the cap. The compliance of the elastomer enables the die and cap to be pressed together without overpressuring the die/circuit board interface. In addition, the high thermal conductivity of the elastomer enables devices having a very high heat output to be cooled to temperatures enabling reliable operation.

[0016] The method of the invention includes steps for forming direct die-to-circuit board connections for "heat sinked" dice as well as for forming "heat sinked" die modules which may be themselves connected to a substrate such as a circuit board.

[0017] These and other features and advantages will be more clearly understood from the following detailed description when taken in conjunction with the accompanying drawings. It is important to note that the illustrations are not necessarily drawn to scale, and that there may be other embodiments of the invention which are not specifically illustrated. Like elements of the various figures are designated by like numerals.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0018] The invention is illustrated in the following figures, wherein:

[0019] FIG. 1 is a perspective view of a wire-bonded Chip On Board (COB) semiconductor device of the invention;

[0020] FIG. 2 is a perspective view of a flip-chip Chip On Board (COB) semiconductor device of the invention;

[0021] FIGS. 3A through 3G are cross-sectional views of a wire-bonded Chip On Board (COB) semiconductor device illustrating the steps of fabrication in accordance with the invention, as taken along line 3-3 of FIG. 1;

[0022] FIGS. 4A through 4F are cross-sectional views of a flip-chip Chip On Board (COB) semiconductor device illustrating the steps of fabrication in accordance with the invention, as taken along line 4-4 of FIG. 2;

[0023] FIG. 5 is a cross-sectional view of a Chip On Board (COB) semiconductor device of the invention having a cap as a heat sink;

[0024] FIG. 6 is a cross-sectional view of a circuit board mounted semiconductor device of the invention having a cap as a heat sink; and

[0025] FIG. 7 is a cross-sectional view of a circuit board mounted semiconductor device of the invention having a heat sink resiliently retained on the semiconductor die.

DETAILED DESCRIPTION OF THE INVENTION

[0026] As shown in drawing FIG. 1, a first semiconductor device 10 with a high heat generation rate is shown. The semiconductor device 10 includes a semiconductor die 12 having an active surface 14 with bond pads 16, as known in the art. The semiconductor die 12 has a back side 18 which is bonded to a substrate 20, shown here as a printed circuit board (PCB). The bond pads 16 are shown as conventionally arrayed near the edges 32 of the semiconductor die 12, and are wire-bonded with conductive, e.g., gold, wires 22 to corresponding electrical connection pads 24 on the substrate 20. Leads on the upper surface 26 and below the upper surface 26 of the substrate 20 are not shown.

[0027] As shown, a heat-conductive heat sink 30 with fins 28 is mounted on the upper, i.e., active surface 14 of the semiconductor die 12, between the rows of bond pads 16. The heat sink 30 has a relatively large exposed surface area, enabling a high transfer rate of thermal energy. An adhesive 34 having a high heat conductance is preferably used, but other adhesives may be alternatively used to bond the heat sink 30 to the semiconductor die 12, particularly because the adhesive 34 is applied in a very thin layer.

[0028] Also shown in drawing FIG. 1 is a "glob top" material 38 applied to encapsulate and seal the semiconductor die 12, wires 22, and surrounding portions 36 of the substrate 20. A major portion of the heat sink 30 is exposed to the ambient air for high heat transfer rates. If necessitated by very high heat generation, a fan (not shown) may be used in the appliance to further increase heat dissipation. The glob top material 38 may be any suitable glob top material, an encapsulant type material, etc.

[0029] In an alternative arrangement, the glob top material 38 may be applied to overcover a major portion or all of the heat sink 30. This results in decreased heat dissipation capability, however, but may be used where the thermal output of the device permits.

[0030] It is evident that more than one semiconductor device 10 may be attached to a single heat sink 30, and together sealed by application of glob top material 38.

[0031] The heat sink 30 is typically formed of a conductive metal such as aluminum, and has one attachment surface 46 which is attachable by adhesive 34 to the semiconductor die 12. The heat sink 30 may be of any design which provides the desired heat dissipation, is joinable to the die active surface 14 and sealable by a glob top material 38. For example, the heat sink 30 may either have fins 28 or be finless.

[0032] Turning now to drawing FIGS. 3A through 3G, the steps of fabricating semiconductor device 10 from a semiconductor die 12, lead wires 22 and a heat sink 30 are outlined in more detail.

[0033] In drawing FIG. 3A, a semiconductor die 12 has an active surface 14 with bond pads 16 near opposing sides of the semiconductor die 12. The back side 18 of the semiconductor die 12 is first bonded to the upper surface 26 of the substrate 20 by a layer of adhesive 40. The substrate 20 may be a printed circuit board (PCB) or other materials such as a flex circuit or ceramic. A layer of a thermally conductive filled gel elastomer 50 may be either applied to the semiconductor die while in wafer form or subsequently applied to active surface 14 between the arrays of bond pads 16 of the semiconductor die 12 after singulation of the semiconductor die 12 from the wafer. The purpose of the gel elastomer 50 is to provide a protective mask over an area of the semiconductor die 12 to which the heat sink 30 (FIG. 3E) is to be bonded. Alternatively, when a second layer is used as a mask, the first layer may be retained on a portion of the semiconductor die 12 after the molding or glob-topping of the semiconductor die 12 for the attachment of a heat sink thereto, if desired (to be described in FIG. 3C). The gel elastomer 50 is applied as a gel or as a semi-solid or solid coupon. The gel elastomer 50, or a suitable silicon elastomeric material, etc. if the gel elastomer 50 is to be disposed after removal from the semiconductor die 12, or the use of a metal filled gel elastomer 50 if such is to remain on the semiconductor die 12, may include one or more dams 52 to help prevent the flow of any

subsequently applied material from covering the surface of the gel elastomer 50. The dams 52 may extend along one or more sides of the semiconductor die 12, as desired, and may be of any suitable height. The dams 52 may be of any suitable material. Alternatively, the dams 52 may comprise a second layer of gel elastomer 50 having a size smaller than that of the gel elastomer 50. Subsequent glob top application is difficult to precisely control, and any glob top material 38 which lands on the gel elastomer 50 will be later removed by removal of the gel elastomer from the active surface 14 of the semiconductor die 12. Typically, the gel elastomer 50 may be removed simply by peeling it from the active surface 14 of the semiconductor die 12. Typically, if the gel elastomer 50 is to be removed from the semiconductor die 12 after the glob top material application, a silicon type elastomer may be used on the semiconductor die 12 and removed therefrom for the application of a heat sink to the semiconductor die 12.

[0034] The gel elastomer 50 is a recently developed material and includes Heat Path™ filled cross-linked silicone gels sold by Raychem. As used in this invention, the gel elastomer 50 is filled with a conductive material to provide high thermal conductivity. The gel elastomer material is compliant under light pressure, has a solid shape retention, cohesive strength and the ability to wet and adhere to surfaces.

[0035] In the next step, shown in drawing FIG. 3B, the bond pads 16 are wire bonded to electrical connection pads 24 on the substrate 20 by, e.g., thermosonic, thermocompression or ultrasonic methods, as known in the art.

[0036] Alternatively, the wire bonding step may precede application of the gel elastomer 50.

[0037] In drawing FIG. 3C, depicted is the next step of the process, that of applying glob top material 38 or suitable potting material to encapsulate the wire connections and the edges 32 (FIG. 3A) of the semiconductor die 12. The glob top material 38 is typically a thermally resistive polymer such as commercially available epoxy or urethane. The glob top material 38 is typically applied as a curable liquid through a small nozzle, not shown, to extend to the layer of gel elastomer 50, or nearly so. As shown, portions 38A and 38B of the glob top material 38 have spilled onto the exposed surface 44 of gel elastomer 50. Without use of the

layer of gel elastomer 50, effective removal of glob top portions 38A and 38B may damage the die semiconductor 12 and/or substrate 20 and/or lead wires 22, etc.

[0038] Application of the glob top material 38 is followed by a curing step, such as by temperature elevation. The glob top material 38 is cured to provide a hard, impenetrable sealing surface.

[0039] As shown in drawing FIG. 3D, the gel elastomer 50 is then peeled away in direction 42 from the active surface 14 of the semiconductor die 12. It has been found that the lower surface 51 of the gel elastomer 50 may be easily and cleanly stripped from the active surface 14 of semiconductor die 12 by simply peeling away the gel elastomer coupon. This leaves the active surface 14 of the semiconductor die 12 clean and prepared for strong bonding of a heat sink 30 with an adhesive 34, shown in drawing FIG. 3E.

[0040] The particular materials which may be used as die-to-substrate adhesives 40 include those commonly known and/or used in the art. Examples of such are polyimides, a 75% silver filled cyanate ester paste, an 80% silver filled cyanate ester paste, a silver filled lead glass paste, etc.

[0041] The adhesive 34 used to bond the heat sink 30 to the active surface 14 of the semiconductor die 12 may be an epoxy or the above identified die-to-substrate adhesives or an adhesive as known in the art.

[0042] As illustrated in drawing FIG. 3F, further glob top material 48 may be applied to the semiconductor device 10, particularly between the existing glob top material 38 and the heat sink 30, for improved sealing. In this figure, the glob top materials 38 and 48 are shown overcovering the substrate 20 between semiconductor device 10 and an adjacent device, of which only a connection pad 24A and a bond wire 22A are visible. The semiconductor device 10 is effectively sealed to the substrate 20 to prevent electrical short-circuiting, wire breakage and debonding, and moisture penetration.

[0043] In drawing FIG. 3G, a semiconductor die 12 has an active surface 14 with bond pads 16 near opposing sides of the semiconductor die 12. The back side 18 (FIG. 4A) of the semiconductor die 12 is first bonded to the upper surface 26 of the substrate 20 by a layer of adhesive 40. The substrate 20 may be a printed circuit board (PCB) or other materials such as a

flex circuit or ceramic. A layer of a thermally conductive filled gel elastomer 50 is either permanently applied to the semiconductor die while in wafer form or subsequently applied to active surface 14 between the arrays of bond pads 16 of the semiconductor die 12 after singulation of the semiconductor die 12 from the wafer. A layer or piece of disposable elastomer or tape 150 is releasably applied over the gel elastomer 50. The purpose of the elastomer or tape 150 is to provide a protective mask over an area of the gel elastomer 50 attached to the semiconductor die 12 to which the heat sink 30 is to be bonded. The elastomer 150 is applied as a semi-solid or solid coupon. The elastomer 150 is to be disposed after removal from the semiconductor die 12 and may include one or more dams 52 to help prevent the flow of any subsequently applied material from covering the surface of the elastomer 150. The dams 52 may extend along one or more sides of the elastomer 150, as desired, and may be of any suitable height. The dams 52 may be of any suitable material. Alternatively, the dams 52 may comprise a second layer of elastomer 150 having a size smaller than that of the gel elastomer 50. Subsequent glob top application is difficult to precisely control, and any glob top material 38 which lands on the elastomer 150 will be later removed by removal of the elastomer 150 from the surface of the gel elastomer 50. Typically, the elastomer 150 may be removed simply by peeling it from the surface of the gel elastomer 50 permanently attached to the semiconductor die 12. Typically, if the elastomer 150 is to be removed from the gel elastomer 50 after the glob top material application, a silicon type elastomer may be used on the semiconductor die 12 and removed therefrom for the application of a heat sink to the semiconductor die 12.

[0044] As shown in drawing FIG. 3G, the layer of elastomer 150 is then peeled away in direction 42 from the surface of the gel elastomer 50. It has been found that the lower surface 152 of the elastomer 150 may be easily and cleanly stripped from the surface of the gel elastomer 50 by simply peeling away the elastomer coupon. This leaves the surface of the gel elastomer 50 clean and prepared for strong bonding of a heat sink 30 with an adhesive 34, shown in drawing FIG. 3E.

[0045] The glob top materials 38 and 48 may be the same or different materials. Glob top materials useful for this application include HYSOL™ FP4451 material or HYSOL™

FP4450 high purity, low stress liquid encapsulant material, available from the DEXTER ELECTRONIC MATERIALS DIVISION OF DEXTER CORPORATION, etc.

[0046] Depicted in drawing FIG. 2 is another aspect of the invention, wherein the semiconductor die 12 is bonded flip-chip fashion to electrical circuit traces 54 on the upper surface 26 of substrate 20. The semiconductor die 12 has an active surface 14 with a grid of electrical connections 56 attached to the corresponding circuit traces 54. The electrical connections 56 may comprise a ball grid array (BGA) of solder balls, as shown, or other array. The opposite, back side 18 of the semiconductor die 12 is directed upwardly, away from the substrate 20. A heat sink 30, here shown with fins 28, has an attachment surface 46 which is adhesively bonded to the back side 18 with adhesive 34. Glob top material 38 is applied to seal the semiconductor die 12, including its edges 32, and a surrounding portion 36 of the substrate. A major portion of the heat sink 30 is exposed to the ambient air for high heat transfer rates. Where very high heat dissipation rates are required, a fan (not shown) may be used to provide a high rate of air movement past the heat sink 30. This type of attachment may similarly be used in chip scale packages, if desired. In such an instance, the semiconductor die 12 would be replaced by a chip scale package bonded flip-chip fashion to electrical circuit traces 54 on the upper surface 26 of substrate 20. The chip scale package has an active surface 14 with a grid of electrical connections 56 attached to the corresponding circuit traces 54. The electrical connections 56 may comprise a ball grid array (BGA) of solder balls, as shown, or other array. The opposite, back side 18 of the chip scale package is directed upwardly, away from the substrate 20. A heat sink 30, here shown with fins 28, has an attachment surface 46 which is adhesively bonded to the back side 18 of the chip scale package with adhesive 34. Glob top material 38 is applied to seal the chip scale package, including its edges 32, and a surrounding portion 36 of the substrate. A major portion of the heat sink 30 is exposed to the ambient air for high heat transfer rates. Where very high heat dissipation rates are required, a fan (not shown) may be used to provide a high rate of air movement past the heat sink 30.

[0047] The steps of fabricating the semiconductor device 10 of drawing FIG. 2 are illustrated in drawing FIGS. 4A through 4F. If a chip scale package is used rather than a

semiconductor die 12, all numerals and descriptions of the invention are the same except that the semiconductor die 12 is a chip scale package.

[0048] As depicted in drawing FIG. 4A, a flip-chip or semiconductor die 12 having an active surface 14 with a grid of electrical connections 56, shown as solder balls, is down bonded to electrical circuit traces 54 (not shown) on an upper surface 26 of a substrate 20. The semiconductor die 12 has an opposing back side 18 and edges 32. The substrate 20 may be a printed circuit board (PCB) or other material such as a flex circuit or ceramic. A layer or coupon of thermally conductive filled gel elastomer 50, alternatively, a suitable elastomer, silicon elastomeric material, etc. if the gel elastomer 50 is to be discarded, is applied as a solid or semisolid to the back side 18 of the semiconductor die 12, either before or (preferably) after the semiconductor die 12 is electrically down bonded to the substrate 20. The gel elastomer 50 masks the back side 18 from glob top material 38 which may be inadvertently misapplied to the back side 18, requiring removal by erosive blasting or other methods. The use of the gel elastomer 50 obviates such glob top removal methods.

[0049] As shown in drawing FIG. 4B, the next step encompasses the application of glob top material 38 to encapsulate and seal the semiconductor die 12 and portions of the adjacent substrate upper surface 26. Preferably, the spaces 60 between the solder balls 56 are first filled with glob top material 38 or another low viscosity polymeric material. In these figures, the glob top material 38 is depicted as applied to form a nearly uniform depth over an extended substrate area. Some of the glob top material 38 is shown as having been misapplied to the layer of gel elastomer 50 as portions 38A and 38B.

[0050] The glob top material 38 is then cured, for example, by heating.

[0051] As shown in drawing FIG. 4C, the gel elastomer 50 is then removed, e.g., by peeling it from the back side 18 of the semiconductor die 12. The back side 18 of semiconductor die 12 in drawing FIG. 4D is then bare and clean for enhanced attachment of a heat sink 30 thereto.

[0052] In drawing FIG. 4E, a heat sink 30 is bonded to the back side 18 of semiconductor die 12 by a layer of adhesive 34, as already described, relative to the embodiment of drawing FIG. 1.

[0053] In drawing FIG. 4F, a further application of a glob top material 48 may be performed, particularly to fill the spaces between the glob top material 38 and the heat sink 30. The glob top material 48 may be the same as glob top material 38, or may be different.

[0054] Alternatively, a room temperature vulcanizing rubber (RTV), which may vary in the degree of thermal conductivity thereof, may be used to completely cover and seal the device to the substrate 20, including the glob top material 38.

[0055] Although a major portion of the heat sink 30 is unencapsulated in the preferred embodiment, the heat sink may also be completely or nearly completely encapsulated.

[0056] The Chip On Board semiconductor device 10 of drawing FIG. 1 or drawing FIG. 2 may be formed as merely one of a plurality of components attached and sealed to a substrate. Alternatively, the chip scale package (CSP) semiconductor device 10, shown in FIG. 6, may be a stand-alone encapsulated device whereby a grid of electrical connections is formed on the opposite side 58 (see FIG. 6) of the substrate 20 for bonding to another substrate, not shown.

[0057] While application of the gel elastomer 50 to the semiconductor die 12, when singulated or while in wafer form, is an additional step in device fabrication, it eliminates the troublesome step of glob top removal required by misapplication of glob top material to the die surface. A clean surface for bonding to a heat sink is assured. In addition, no other layers of good conductors and/or poor conductors are required, enabling both (a) high heat removal and (b) a device of reduced dimensions.

[0058] The gel elastomer 50 may also be used as a permanent compliant member 70 between a semiconductor die 12 and a heat sink 30. As depicted in drawing FIG. 5, a semiconductor die 12 has an active surface 14 with a ball grid array (BGA) of electrical connections 56 connected to traces (not shown) on a circuit board or other substrate 20. A layer 70 of gel elastomer is then applied to inside attachment surface 46 of a cap style heat sink 30. The heat sink 30 may be finned, or have no fins 28. In one embodiment, the heat sink 30 has lateral walls 62 whose lower edges 64 are designed to abut the upper surface 26 of the substrate 20. Alternatively (FIG. 6), a portion of the substrate 20 is configured to fit within the open end 66 of the heat sink 30.

[0059] As depicted in drawing FIG. 7, a semiconductor die 12 has an active surface 14 with a ball grid array (BGA) of electrical connections 56 connected to traces (not shown) on a circuit board or other substrate 20 having a plurality of apertures 21 therein. A layer 70 of gel elastomer is then applied to inside attachment surface 46 of a cap style heat sink 30. The heat sink 30 may be finned, or have no fins 28. In one embodiment, the heat sink 30 has resilient spring members 31 having a portion thereof engaging a fin 28 while the other end thereof engages an aperture 21 of the substrate 20 to resiliently retain the heat sink 30 engaging the gel elastomer layer 70 which engages the back side 18 of the semiconductor die 12, leaving the heat sink 30 and semiconductor die 12 free to move with respect to each other.

[0060] In either case, as illustrated in drawing FIGS. 5, 6, and 7, the back side 18 of semiconductor die 12 is then pressed into the gel elastomer layer 70 for attachment thereto. The adhesion of the gel elastomer layer 70 to the attachment surface 46 of the heat sink 30 and the back side 18 of the semiconductor die 12 as well as the resilient spring members 31 holds the parts in place.

[0061] As a further step, the interior of the heat sink "cap" may be filled with encapsulant material 68 as shown in FIG. 6. In the embodiment of drawing FIG. 5, encapsulant may be injected through holes (not shown) in the heat sink 30.

[0062] The embodiment of drawing FIG. 6 is shown with a further ball grid array (BGA) of solder balls 72 on the opposite side 58 of the substrate. Thus, the semiconductor device 10 may be bonded to another substrate, such as a circuit board, not shown.

[0063] In an alternative method of forming the semiconductor devices of drawing FIGS. 5 and 6, the gel elastomer layer 70 is first applied to back side 18 of the semiconductor die 12, which is then pressed into the attachment surface 46 of the heat sink 30.

[0064] In the embodiments of drawing FIGS. 5 and 6, overpressuring of the die/substrate interface is eliminated by the compliance of the filled gel elastomer. Simultaneously, the high thermal conductivity of the filled gel elastomer maintains high heat dissipation from the device.

[0065] It is apparent to those skilled in the art that various changes and modifications may be made to the method and apparatus of the invention as disclosed herein without departing from the spirit and scope of the invention as defined in the following claims.

ABSTRACT OF THE DISCLOSURE

A process for forming a thermally enhanced Chip On Board semiconductor device with a heat sink is described. In one aspect, a thermally conducting filled gel elastomer material or a silicon elastomeric material or elastomeric material, if the material is to be removed, is applied to the die surface to which the heat sink is to be bonded. During the subsequent glob top application and curing steps, difficult-to-remove glob top material which otherwise may be misapplied to the die surface adheres to the upper surface of the elastomer material. The elastomer material is removed by peeling prior to adhesion bonding of the heat sink to the die. In another aspect, the thermally conducting filled gel elastomer material is applied between a die surface and the inside attachment surface of a cap-style heat sink to eliminate overpressure on the die/substrate interface.

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APPENDIX B

(VERSION OF SUBSTITUTE SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE)

(Serial No. 09/834,297)

PATENT
Attorney Docket 3592.5US (97-321.5)

NOTICE OF EXPRESS MAILING

Express Mail Mailing Label Number:_____

Date of Deposit with USPS: _____

Person making Deposit: _____

APPLICATION FOR LETTERS PATENT

for

CHIP ON BOARD WITH HEAT SINK ATTACHMENT AND ASSEMBLY

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CHIP ON BOARD WITH HEAT SINK ATTACHMENT AND ASSEMBLY

BACKGROUND OF THE INVENTION

[0001] ~~Cross-Reference to Related Applications~~Cross-Reference to Related Applications: This application is a continuation of application Serial No. 09/510,894, filed February 23, 2000, now U.S. Patent 6,229,204 B1, issued May 8, 2001, which is a divisional of application Serial No. 09/146,945, filed September 3, 1998, now U.S. Patent 6,117,797, issued September 12, 2000.

[0002] ~~Field of the Invention~~Field of the Invention: This invention relates generally to integrated circuit packages and methods of package assembly. More particularly, the present invention pertains to the manufacture of Chip On Board devices with heat sinks for high power dissipation.

[0003] ~~State of the Art~~State of the Art: Semiconductor devices are used in a wide variety of products, including computers, automobiles, integrated circuit cards, audio/video products, and a plethora of other electronic apparatus.

[0004] Modern electronic appliances such as computers have hundreds of integrated circuits (IC) and other electronic components, most of which are mounted on printed circuit boards (PCB). Heat is generated by such components. The heat generated by many ICs and other electronic components with simple circuits may often be dissipated without an additional heat sink. However, components requiring added heat sinks are becoming more numerous as the required speed, circuit complexity, and circuit density have increased.

[0005] In particular, as semiconductor devices have become more dense in terms of electrical power consumption per unit volume, heat generation has greatly increased, requiring package construction which dissipates the generated heat much more rapidly. As the state of the art progresses, the ability to adequately dissipate heat is often a severe constraint on the size, speed, and power consumption of an integrated circuit design.

[0006] The term "heat sink" is used herein in general reference to a passive heat transfer device, for example, an extruded aluminum plate with or without fins thereon. The plate is thermally coupled to an electronic component, ~~e.g.~~ e.g., semiconductor die, to absorb heat

from the component and dissipate the heat by convection into the air. In this application, a heat sink will be distinguished from a "heat ~~spreader",~~ spreader," the latter pertaining to a member which channels heat from a semiconductor die to leads which exit the die package. However, a heat sink and a heat spreader may together be used to cool a device.

[0007] Integrated circuit devices are constructed by ~~making e.g.~~ making, e.g., a (silicon or germanium) semiconductor die with internal and surface circuits including transistors, resistors, capacitors, etc. A single semiconductor die may contain thousands of such components and generate considerable heat. Electrical connection pads on an "active" surface of the semiconductor die are connected to the various die circuits. The integrated circuit device also includes electrical leads enabling the electrical connection pads of the semiconductor die to be connected to circuits on a ~~printed circuit board (PCB)~~ PCB (or other substrate) of an appliance.

[0008] Dissipation of generated thermal energy is necessary for safe operation of an electronic appliance. An excessively high temperature of an IC may cause a circuit board fire and damage or destroy the appliance. High temperatures cause failure of the integrated circuits themselves. State of the art methods for absorbing and dissipating thermal energy from high speed Chip On Board (COB) semiconductor devices are inadequate for any or all of the following reasons: (a) insufficient heat transfer capability, (b) excessively large package size, especially the profile height, (c) complexity of manufacture, and/or (d) excessive cost.

[0009] Current methods of forming glob topped Chip On Board devices with heat sinks are shown in United States Patent 5,552,635 of Kim et al., United States Patent 5,477,082 of Buckley III et al., United States Patent 5,468,995 of Higgins III, United States Patent 5,610,442 of Schneider et al., and United States Patent 5,659,952 of Kovac et al.

[0010] In United States Patent 5,450,283 of Lin et al., a method for making a semiconductor device with an exposed die back side is described. The method includes providing a printed wiring board (PWB) substrate with conductive traces, on which a semiconductor die is flip mounted and connected to the conductive traces. An electrically ~~non-conductive~~ nonconductive coupling material is placed between the die and substrate. A package body is formed around the perimeter of the die, covering a portion of the conductive traces and any portion of the coupling material extending beyond the die perimeter. The back

side of the die is left exposed through the use of a thin layer of tape placed in the mold cavity prior to the transfer molding of the package body around the die to prevent the flow of molding material forming the package from flowing on the inactive back side of the die. If the thin layer of tape adheres to the die after removal of the semiconductor device from the mold cavity, the thin layer of tape is removed from the die of the semiconductor device.

[0011] A device made with multiple layers of encapsulant is shown in United States Patent 5,379,186 of Gold et al.

SUMMARY OF THE INVENTION

[0012] In accordance with the invention, an improved method for fabricating a Chip On Board semiconductor device requiring enhanced heat dissipation is applicable to direct attachment of semiconductor devices, such as dynamic memory semiconductor dice, to substrates, such as circuit boards and the like, and to the formation of modules incorporating a substrate, such as a circuit board.

[0013] In one aspect of the invention, an elastomer is used to cover a portion of a semiconductor die prior to glob top application of the die to the circuit board. The elastomer is removed, ~~e.g.~~ e.g., by peeling, from the die surface and includes any glob top material which has inadvertently been applied to the elastomer. Thus, the portion of the semiconductor die remains free of contaminants. If desired, since a portion of the semiconductor die is free of contaminants, providing a good adhesion surface, a heat sink may be attached to such portion of the semiconductor die. The method is applicable to both wire-bonded ~~dies~~ dice and flip-chip die bonding to circuit boards. ~~Alternately,~~ Alternatively, the elastomer may be retained on a portion of the semiconductor die after the molding or glob-topping of the die for the attachment of a heat sink thereto, if desired. The elastomer may be a highly thermally conductive elastomer to enhance the heat transfer from the semiconductor die to the surrounding environment. An example of a highly thermally conductive elastomer is a metal-filled elastomer or an elastomer filled with a highly thermally conductive material like metal.

[0014] The preferred elastomer is highly heat conductive, very compliant, has a relatively low adhesiveness and a high surface wetting property, all the type of properties that enhances heat transfer from the semiconductor die.

[0015] In another aspect of the invention, a heat conductive cap is formed over a semiconductor die and comprises a heat sink. A layer of the metal filled gel elastomer is placed between the non-active surface of a die and the cap. Compressing the die into the cap forms the desired adhesion to retain the die within the cap. The compliance of the elastomer enables the die and cap to be pressed together without overpressuring the die/circuit board interface. In addition, the high thermal conductivity of the elastomer enables devices having a very high heat output to be cooled to temperatures enabling reliable operation.

[0016] The method of the invention includes steps for forming direct die-to-circuit board connections for "heat ~~sinked dies"~~ sinked" dice as well as for forming "heat sinked" die modules which may be themselves connected to a substrate such as a circuit board.

[0017] These and other features and advantages will be more clearly understood from the following detailed description when taken in conjunction with the accompanying drawings. It is important to note that the illustrations are not necessarily drawn to scale, and that there may be other embodiments of the invention which are not specifically illustrated. Like elements of the various figures are designated by like numerals.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWINGS

[0018] The invention is illustrated in the following figures, wherein:

[0019] FIG. 1 is a perspective view of a wire-bonded Chip On Board (COB) semiconductor device of the invention;

[0020] FIG. 2 is a perspective view of a flip-chip Chip On Board (COB) semiconductor device of the invention;

[0021] FIGS. 3A through 3G are cross-sectional views of a wire-bonded Chip On Board (COB) semiconductor device illustrating the steps of fabrication in accordance with the invention, as taken along line 3-3 of FIG. 1;

[0022] FIGS. 4A through 4F are cross-sectional views of a flip-chip Chip On Board (COB) semiconductor device illustrating the steps of fabrication in accordance with the invention, as taken along line 4-4 of FIG. 2;

[0023] FIG. 5 is a cross-sectional view of a Chip On Board (COB) semiconductor device of the invention having a cap as a heat sink;

[0024] FIG. 6 is a cross-sectional view of a circuit board mounted semiconductor device of the invention having a cap as a heat sink; and

[0025] FIG. 7 is a cross-sectional view of a circuit board mounted semiconductor device of the invention having a heat sink resiliently retained on the semiconductor die.

DETAILED DESCRIPTION OF THE INVENTION

[0026] As shown in drawing FIG. 1, a first semiconductor device 10 with a high heat generation rate is shown. The semiconductor device 10 includes a semiconductor die 12 having an active surface 14 with bond pads 16, as known in the art. The semiconductor die 12 has a back side 18 which is bonded to a substrate 20, shown here as a printed circuit board (PCB). The bond pads 16 are shown as conventionally arrayed near the edges 32 of the semiconductor die 12, and are wire-bonded with conductive, ~~e.g.~~ e.g., gold, wires 22 to corresponding electrical connection pads 24 on the substrate 20. Leads on the upper surface 26 and below the upper surface 26 of the substrate 20 are not shown.

[0027] As shown, a heat-conductive heat sink 30 with fins 28 is mounted on the upper, ~~i.e.~~ i.e., active surface 14 of the semiconductor die 12, between the rows of bond pads 16. The heat sink 30 has a relatively large exposed surface area, enabling a high transfer rate of thermal energy. An adhesive 34 having a high heat conductance is preferably used, but other adhesives may be alternatively used to bond the heat sink 30 to the semiconductor die 12, particularly because the adhesive 34 is applied in a very thin layer.

[0028] Also shown in drawing FIG. 1 is a "glob top" material 38 applied to encapsulate and seal the semiconductor die 12, wires 22, and surrounding portions 36 of the substrate 20. A major portion of the heat sink 30 is exposed to the ambient air for high heat transfer rates. If necessitated by very high heat generation, a fan (not shown) may be used in the appliance to

further increase heat dissipation. The glob top material 38 may be any suitable glob top material, an encapsulant type material, etc.

[0029] In an alternative arrangement, the glob top material 38 may be applied to overcover a major portion or all of the heat sink 30. This results in decreased heat dissipation capability, however, but may be used where the thermal output of the device permits.

[0030] It is evident that more than one semiconductor device 10 may be attached to a single heat sink 30, and together sealed by application of glob top material 38.

[0031] The heat sink 30 is typically formed of a conductive metal such as aluminum, and has one attachment surface 46 which is attachable by adhesive 34 to the semiconductor die 12. The heat sink 30 may be of any design which provides the desired heat dissipation, is joinable to the die active surface 14 and sealable by a glob top material 38. For example, the heat sink 30 may either have fins 28 or be finless.

[0032] Turning now to drawing FIGS. 3A through 3G, the steps of fabricating semiconductor device 10 from a semiconductor die 12, lead wires 22 and a heat sink 30 are outlined in more detail.

[0033] In drawing FIG. 3A, a semiconductor die 12 has an active surface 14 with bond pads 16 near opposing sides of the semiconductor die 12. The back side 18 of the semiconductor die 12 is first bonded to the upper surface 26 of the substrate 20 by a layer of adhesive 40. The substrate 20 may be a printed circuit board (PCB) or other materials such as a flex circuit or ceramic. A layer of a thermally conductive filled gel elastomer 50 may be either applied to the semiconductor die while in wafer form or subsequently applied to active surface 14 between the arrays of bond pads 16 of the ~~die~~ semiconductor die 12 after singulation of the semiconductor die 12 from the wafer. The purpose of the gel elastomer 50 is to provide a protective mask over an area of the semiconductor die 12 to which the heat sink 30 (FIG. 3E) is to be bonded. ~~Alternately,~~ Alternatively, ~~the elastomer~~ when a second layer is used as a mask, the first layer may be retained on a portion of the semiconductor die 12 after the molding or glob-topping of the semiconductor die 12 for the attachment of a heat sink thereto, if desired (to be described in FIG. 3C). The gel elastomer 50 is applied as a gel or as a semi-solid or solid coupon. The gel elastomer 50, or a suitable silicon elastomeric material, etc. if the gel elastomer 50 is to be

disposed after removal from the semiconductor die 12, or the use of a metal filled gel elastomer 50 if such is to remain on the semiconductor die 12, may include one or more dams 52 to help prevent the flow of any subsequently applied material from covering the surface of the gel elastomer 50. The dams 52 may extend along one or more sides of the semiconductor die 12, as desired, and may be of any suitable height. The dams 52 may be of any suitable material. ~~Alternately,~~ Alternatively, the dams 52 may comprise a second layer of gel elastomer 50 having a size smaller than that of the gel elastomer 50. Subsequent glob top application is difficult to precisely control, and any glob top material 38 which lands on the gel elastomer 50 will be later removed by removal of the gel elastomer from the active surface 14 of the semiconductor die 12. Typically, the gel elastomer 50 may be removed simply by peeling it from the active surface 14 of the semiconductor die 12. Typically, if the gel elastomer 50 is to be removed from the semiconductor die 12 after the glob top material application, a silicon type elastomer may be used on the semiconductor die 12 and removed therefrom for the application of a heat sink to the semiconductor die 12.

[0034] The gel elastomer 50 is a recently developed material and includes Heat Path™ filled cross-linked silicone gels sold by Raychem. As used in this invention, the gel elastomer 50 is filled with a conductive material to provide high thermal conductivity. The gel elastomer material is compliant under light pressure, has a solid shape retention, cohesive strength and the ability to wet and adhere to surfaces.

[0035] In the next step, shown in drawing FIG. 3B, the bond pads 16 are ~~wirebonded~~ wire bonded to electrical connection pads 24 on the substrate 20 ~~by e.g.~~ by, e.g., thermosonic, thermocompression or ultrasonic methods, as known in the art.

[0036] Alternatively, the wire bonding step may precede application of the gel elastomer 50.

[0037] In drawing FIG. 3C, depicted is the next step of the process, that of applying glob top material 38 or suitable potting material to encapsulate the wire connections and the edges 32 (FIG. 3A) of the semiconductor die 12. The glob top material 38 is typically a thermally resistive polymer such as commercially available epoxy or urethane. The glob top material 38 is typically applied as a curable liquid through a small nozzle, not shown, to extend

to the layer of gel elastomer 50, or nearly so. As shown, portions 38A and 38B of the glob top material 38 have spilled onto the exposed surface 44 of gel elastomer 50. Without use of the layer of gel elastomer 50, effective removal of glob top portions 38A and 38B may damage the die semiconductor 12 and/or substrate 20 and/or lead wires 22, etc.

[0038] Application of the glob top material 38 is followed by a curing step, such as by temperature elevation. The glob top material 38 is cured to provide a hard, impenetrable sealing surface.

[0039] As shown in drawing FIG. 3D, the gel elastomer 50 is then peeled away in direction 42 from the active surface 14 of the semiconductor die 12. It has been found that the lower surface 51 of the gel elastomer 50 may be easily and cleanly stripped from the active surface 14 of semiconductor die 12 by simply peeling away the gel elastomer coupon. This leaves the active surface 14 of the semiconductor die 12 clean and prepared for strong bonding of a heat sink 30 with an adhesive 34, shown in drawing FIG. 3E.

[0040] The particular materials which may be used as die-to-substrate adhesives 40 include those commonly known and/or used in the art. Examples of such are polyimides, a 75% silver filled cyanate ester paste, an 80% silver filled cyanate ester paste, a silver filled lead glass paste, ~~a silver filled cyanate ester paste,~~ etc.

[0041] The adhesive 34 used to bond the heat sink 30 to the active surface 14 of the semiconductor die 12 may be an epoxy or the above identified die-to-substrate adhesives or an adhesive as known in the art.

[0042] As illustrated in drawing FIG. 3F, further glob top material 48 may be applied to the semiconductor device 10, particularly between the existing glob top material 38 and the heat sink 30, for improved sealing. In this figure, the glob top materials 38 and 48 are shown overcovering the substrate 20 between semiconductor device 10 and an adjacent device, of which only a connection pad 24A and a bond wire 22A are visible. The semiconductor device 10 is effectively sealed to the substrate 20 to prevent electrical short-circuiting, wire breakage and debonding, and moisture penetration.

[0043] In drawing FIG. 3G, a semiconductor die 12 has an active surface 14 with bond pads 16 near opposing sides of the semiconductor die 12. The back side 18 (FIG. 4A) of the

semiconductor die 12 is first bonded to the upper surface 26 of the substrate 20 by a layer of adhesive 40. The substrate 20 may be a printed circuit board (PCB) or other materials such as a flex circuit or ceramic. A layer of a thermally conductive filled gel elastomer 50 is either permanently applied to the semiconductor die while in wafer form or subsequently applied to active surface 14 between the arrays of bond pads 16 of the semiconductor die 12 after singulation of the semiconductor die 12 from the wafer. A layer or piece of disposable elastomer or tape 150 is releasably applied over the gel elastomer 50. The purpose of the elastomer or tape 150 is to provide a protective mask over an area of the gel elastomer 50 attached to the semiconductor die 12 to which the heat sink 30 is to be bonded. The elastomer 150 is applied as a semi-solid or solid coupon. The elastomer 150 is to be disposed after removal from the semiconductor die 12 and may include one or more dams 52 to help prevent the flow of any subsequently applied material from covering the surface of the elastomer 150. The dams 52 may extend along one or more sides of the elastomer 150, as desired, and may be of any suitable height. The dams 52 may be of any suitable material. ~~Alternately,~~ Alternatively, the dams 52 may comprise a second layer of ~~gel~~ elastomer ~~material~~ 150 having a size smaller than that of the gel elastomer ~~material~~ 50. Subsequent glob top application is difficult to precisely control, and any glob top material 38 which lands on the elastomer 150 will be later removed by removal of the elastomer 150 from the surface of the gel elastomer 50. Typically, the elastomer 150 may be removed simply by peeling it from the surface of the gel elastomer ~~150~~ 50 permanently attached to the semiconductor die 12. Typically, if the elastomer 150 is to be removed from the gel elastomer 50 after the glob top material application, a silicon type elastomer may be used on the semiconductor die 12 and removed therefrom for the application of a heat sink to the semiconductor die 12.

[0044] As shown in drawing FIG. 3G, the layer of elastomer 150 is then peeled away in direction 42 from the surface of the gel elastomer 50. It has been found that the lower surface 152 of the elastomer 150 may be easily and cleanly stripped from the surface of the gel elastomer 50 by simply peeling away the elastomer coupon. This leaves the surface of the gel elastomer 50 clean and prepared for strong bonding of a heat sink 30 with an adhesive 34, shown in drawing FIG. 3E.

[0045] The glob top materials 38 and 48 may be the same or different materials. Glob top materials useful for this application include HYSOL™ FP4451 material or HYSOL™ FP4450 high purity, low stress liquid encapsulant material, available from the DEXTER ELECTRONIC MATERIALS DIVISION OF DEXTER CORPORATION, etc.

[0046] Depicted in drawing FIG. 2 is another aspect of the invention, wherein the semiconductor die 12 is bonded ~~flip chip~~ flip-chip fashion to electrical circuit traces 54 on the upper surface 26 of substrate 20. The semiconductor die 12 has an active surface 14 with a grid of electrical connections 56 attached to the corresponding circuit traces 54. The electrical connections 56 may comprise a ball grid array (BGA) of solder balls, as shown, or other array. The opposite, back side 18 of the semiconductor die 12 is directed upwardly, away from the substrate 20. A heat sink 30, here shown with fins 28, has an attachment surface 46 which is adhesively bonded to the back side 18 with adhesive 34. Glob top material 38 is applied to seal the semiconductor die 12, including its edges 32, and a surrounding portion 36 of the substrate. A major portion of the heat sink 30 is exposed to the ambient air for high heat transfer rates. Where very high heat dissipation rates are required, a fan (not shown) may be used to provide a high rate of air movement past the heat sink 30. This type of attachment may similarly be used in chip scale packages, if desired. In such an instance, the semiconductor die 12 would be replaced by a chip scale package ~~12' bonded flip chip~~ bonded flip-chip fashion to electrical circuit traces 54 on the upper surface 26 of substrate 20. The chip scale package ~~12' having~~ has an active surface 14 with a grid of electrical connections 56 attached to the corresponding circuit traces 54. The electrical connections 56 may comprise a ball grid array (BGA) of solder balls, as shown, or other array. The opposite, back side 18 of the chip scale package ~~12' being~~ is directed upwardly, away from the substrate 20. A heat sink 30, here shown with fins 28, has an attachment surface 46 which is adhesively bonded to the back side 18 of the chip scale package with adhesive 34. Glob top material 38 is applied to seal the chip scale ~~package 12',~~ package, including its edges 32, and a surrounding portion 36 of the substrate. A major portion of the heat sink 30 is exposed to the ambient air for high heat transfer rates. Where very high heat dissipation rates are required, a fan (not shown) may be used to provide a high rate of air movement past the heat sink 30.

[0047] The steps of fabricating the semiconductor device 10 of drawing FIG. 2 are illustrated in drawing FIGS. 4A through 4F. If a chip scale package is used rather than a semiconductor die 12, all numerals and descriptions of the invention are the same except that the semiconductor die 12 is a chip scale package.

[0048] As depicted in drawing FIG. 4A, a ~~flip chip~~ flip-chip or semiconductor die 12 having an active surface 14 with a grid of electrical connections ~~56~~56, shown as solder ~~balls~~ balls, is down bonded to electrical circuit traces 54 (not shown) ~~on~~on an upper surface 26 of a substrate 20. The semiconductor die 12 has an opposing back side 18 and edges 32. The substrate 20 may be a printed circuit board (PCB) or other material such as a flex circuit or ceramic. A layer or coupon of thermally conductive filled gel elastomer 50, ~~alternately~~ alternatively, a suitable elastomer, silicon elastomeric material, etc. if the gel elastomer 50 is to be discarded, is applied as a solid or semisolid to the back side 18 of the semiconductor die 12, either before or (preferably) after the semiconductor die 12 is electrically down bonded to the substrate 20. The gel elastomer 50 masks the back side 18 from glob top material 38 which may be inadvertently misapplied to the back side 18, requiring removal by erosive blasting or other methods. The use of the gel elastomer 50 obviates such glob top removal methods.

[0049] As shown in drawing FIG. 4B, the next step encompasses the application of glob top material 38 to encapsulate and seal the semiconductor die 12 and portions of the adjacent substrate upper surface 26. Preferably, the spaces 60 between the solder balls 56 are first filled with glob top material 38 or another low viscosity polymeric material. In these figures, the glob top material 38 is depicted as applied to form a nearly uniform depth over an extended substrate area. Some of the glob top material 38 is shown as having been misapplied to the layer of gel elastomer 50 as portions 38A and 38B.

[0050] The glob top material 38 is then cured, for example, by heating.

[0051] As shown in drawing FIG. 4C, the gel elastomer 50 is then ~~removed e.g.~~ removed, e.g., by peeling it from the back side 18 of the semiconductor die 12. The back side 18 of semiconductor die 12 in drawing FIG. 4D is then bare and clean for enhanced attachment of a heat sink 30 thereto.

[0052] In drawing FIG. 4E, a heat sink 30 is bonded to the back side 18 of semiconductor die 12 by a layer of adhesive 34, as already ~~described~~ described, relative to the embodiment of drawing FIG. 1.

[0053] ~~A~~ In drawing FIG. 4F, a further application of a glob top material 48 may be performed, particularly to fill the spaces between the glob top material 38 and the heat sink 30. The glob top material 48 may be the same as glob top material 38, or may be different.

[0054] Alternatively, a room temperature vulcanizing rubber ~~(RTV)~~ (RTV), which may vary in the degree of thermal conductivity ~~thereof~~ thereof, may be used to completely cover and seal the device to the substrate 20, including the glob top material 38.

[0055] Although a major portion of the heat sink 30 is unencapsulated in the preferred embodiment, the heat sink may also be completely or nearly completely encapsulated.

[0056] The Chip On Board semiconductor device 10 of drawing FIG. 1 or drawing FIG. 2 may be formed as merely one of a plurality of components attached and sealed to a substrate. Alternatively, the chip scale package (CSP) semiconductor device 10, shown in FIG. 6, may be a stand-alone encapsulated device whereby a grid of electrical connections is formed on the opposite side 58 (see FIG. 6) of the substrate 20 for bonding to another substrate, not shown.

[0057] While application of the gel elastomer 50 to the semiconductor die 12, when singulated or while in wafer form, is an additional step in device fabrication, it eliminates the troublesome step of glob top removal required by misapplication of glob top material to the die surface. A clean surface for bonding to a heat sink is assured. In addition, no other layers of good conductors and/or poor conductors are required, enabling both (a) high heat removal and (b) a device of reduced dimensions.

[0058] The gel elastomer 50 may also be used as a permanent compliant member 70 between a semiconductor die 12 and a heat sink 30. As depicted in drawing FIG. 5, a semiconductor die 12 has an active surface 14 with a ball grid array (BGA) of ~~solder balls~~ electrical connections 56 connected to traces (not shown) on a circuit board or other substrate 20. A layer 70 of gel elastomer is then applied to inside attachment surface 46 of a cap style heat sink 30. The heat sink 30 may be finned, or have no fins 28. In one embodiment, the heat sink 30

has lateral walls 62 whose lower edges 64 are designed to abut the upper surface 26 of the substrate 20. Alternatively (FIG. 6), a portion of the substrate 20 is configured to fit within the open end 66 of the heat sink 30.

[0059] As depicted in drawing FIG. 7, a semiconductor die 12 has an active surface 14 with a ball grid array (BGA) of ~~solder balls~~ electrical connections 56 connected to traces (not shown) on a circuit board or other substrate 20 having a plurality of apertures 21 therein. A layer 70 of gel elastomer is then applied to inside attachment surface 46 of a cap style heat sink 30. The heat sink 30 may be finned, or have no fins 28. In one embodiment, the heat sink 30 has resilient spring members 31 having a portion thereof engaging a fin 28 while the other end thereof engages an aperture 21 of the substrate 20 to resiliently retain the heat sink 30 engaging the ~~layer of~~ gel elastomer layer 70 which engages the back side 18 of the semiconductor die 12, leaving the heat sink 30 and semiconductor die 12 free to move with respect to each other.

[0060] In either case, as illustrated in drawing FIGS. 5, 6, and 7, the back side 18 of semiconductor die 12 is then pressed into the gel elastomer layer 70 for attachment thereto. The adhesion of the gel elastomer layer 70 to the attachment surface 46 of the heat sink 30 and the back side 18 of the semiconductor die 12 as well as the resilient spring members 31 holds the parts in place.

[0061] As a further step, the interior of the heat sink "cap" may be filled with encapsulant material 68 as shown in FIG. 6. In the embodiment of drawing FIG. 5, encapsulant may be injected through holes (not shown) in the heat sink 30.

[0062] The embodiment of drawing FIG. 6 is shown with a further ball grid array (BGA) of solder balls 72 on the ~~exterior surface~~ opposite side 58 of the substrate. Thus, the semiconductor device 10 may be bonded to another ~~substrate~~ substrate, such as a circuit board, not shown.

[0063] In an ~~alternate~~ alternative method of forming the semiconductor devices of drawing FIGS. 5 and 6, the gel elastomer layer 70 is first applied to back side 18 of the semiconductor die 12, which is then pressed into the attachment surface 46 of the heat sink 30.

[0064] In the embodiments of drawing FIGS. 5 and 6, overpressuring of the die/substrate interface is eliminated by the compliance of the filled gel elastomer.

Simultaneously, the high thermal conductivity of the filled gel elastomer maintains high heat dissipation from the device.

[0065] It is apparent to those skilled in the art that various changes and modifications may be made to the method and apparatus of the invention as disclosed herein without departing from the spirit and scope of the invention as defined in the following claims.

ABSTRACT OF THE DISCLOSURE

A process for forming a thermally enhanced Chip On Board semiconductor device with a heat sink is described. In one aspect, a thermally conducting filled gel elastomer material or a silicon elastomeric material or elastomeric material, if the material is to be removed, is applied to the die surface to which the heat sink is to be bonded. During the subsequent glob top application and curing steps, difficult-to-remove glob top material which otherwise may be misapplied to the die surface adheres to the upper surface of the elastomer material. The elastomer material is removed by peeling prior to adhesion bonding of the heat sink to the die. In another aspect, the thermally conducting filled gel elastomer material is applied between a die surface and the inside attachment surface of a cap-style heat sink to eliminate overpressure on the die/substrate interface.

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APPENDIX C

(REPLACEMENT SHEETS AND ANNOTATED SHEETS SHOWING CHANGES)

(Serial No. 09/834,297)

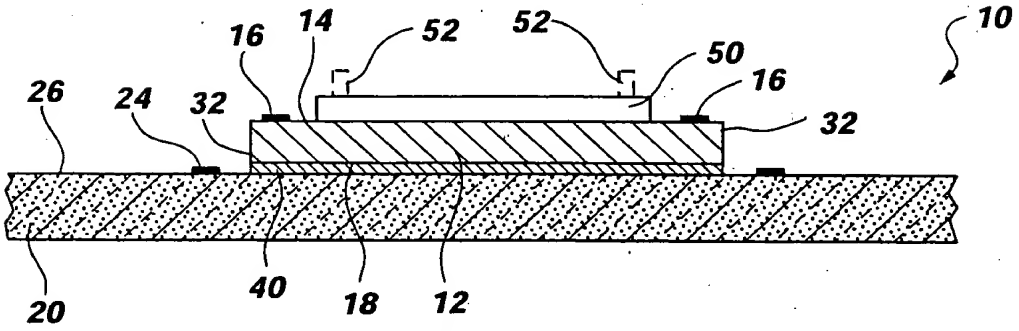

Fig. 3A

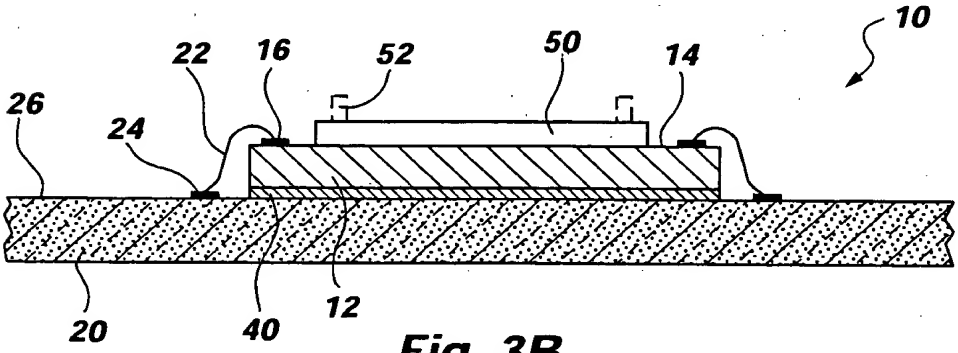

Fig. 3B

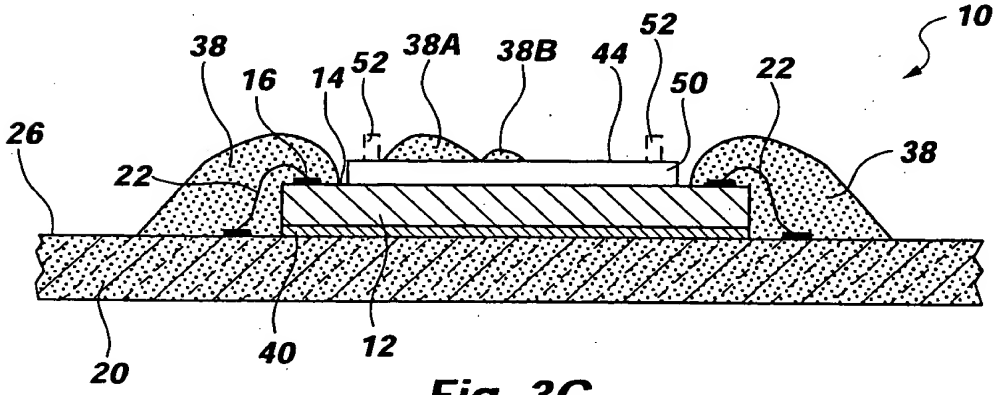

Fig. 3C

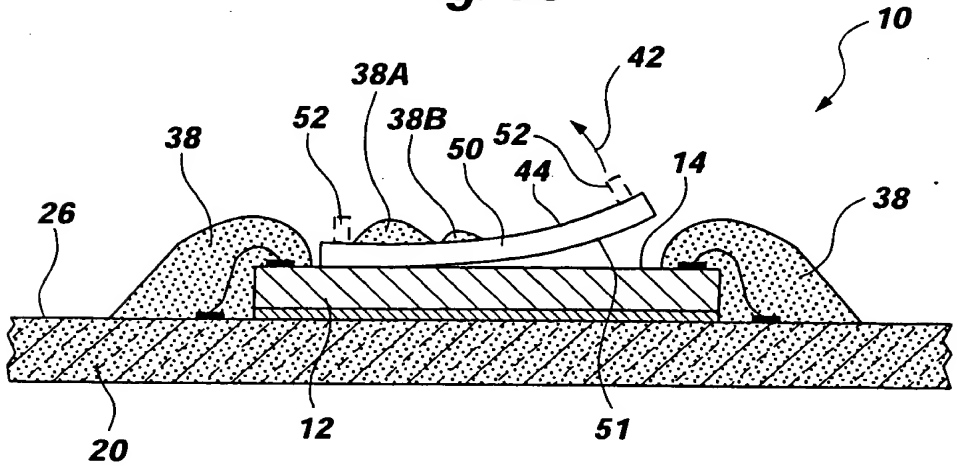

Fig. 3D

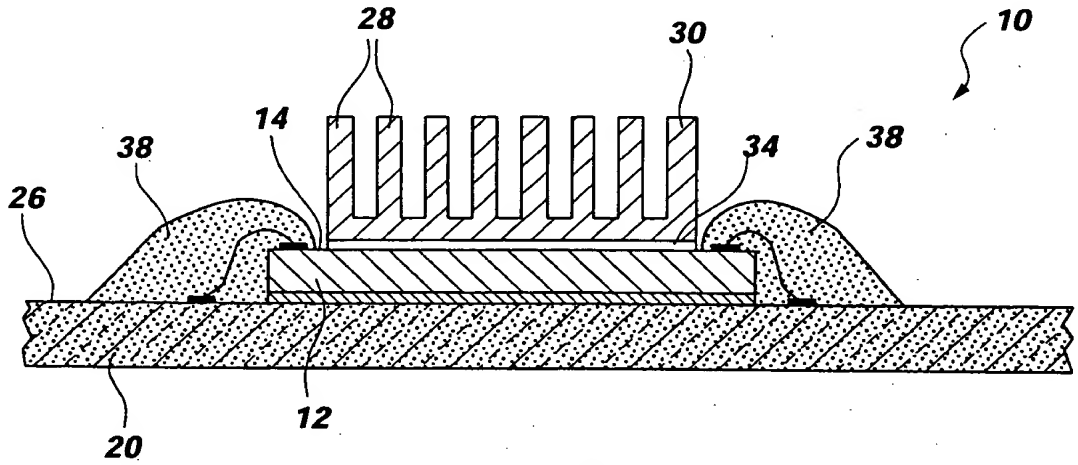

Fig. 3E

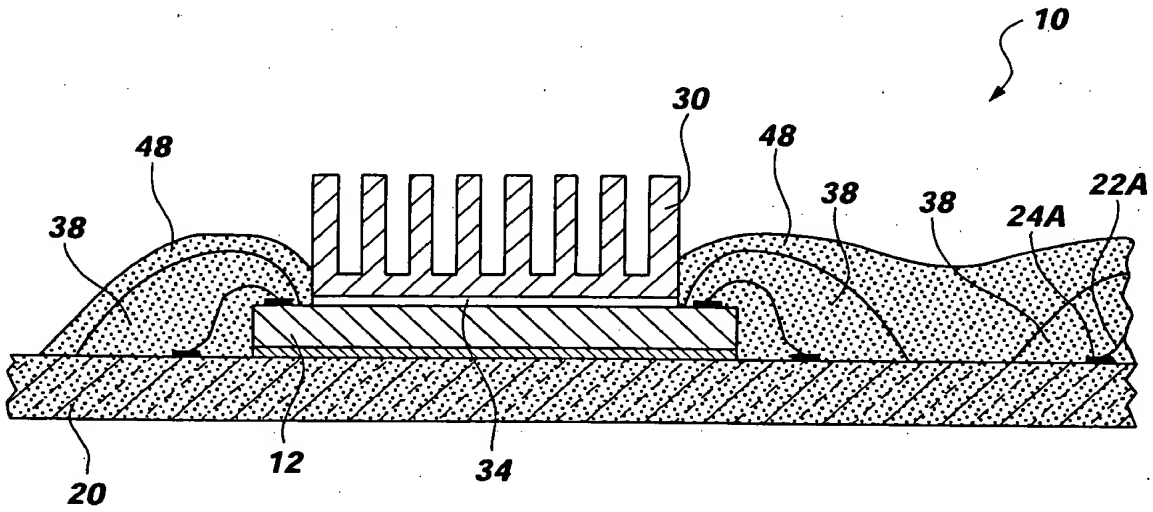

Fig. 3F

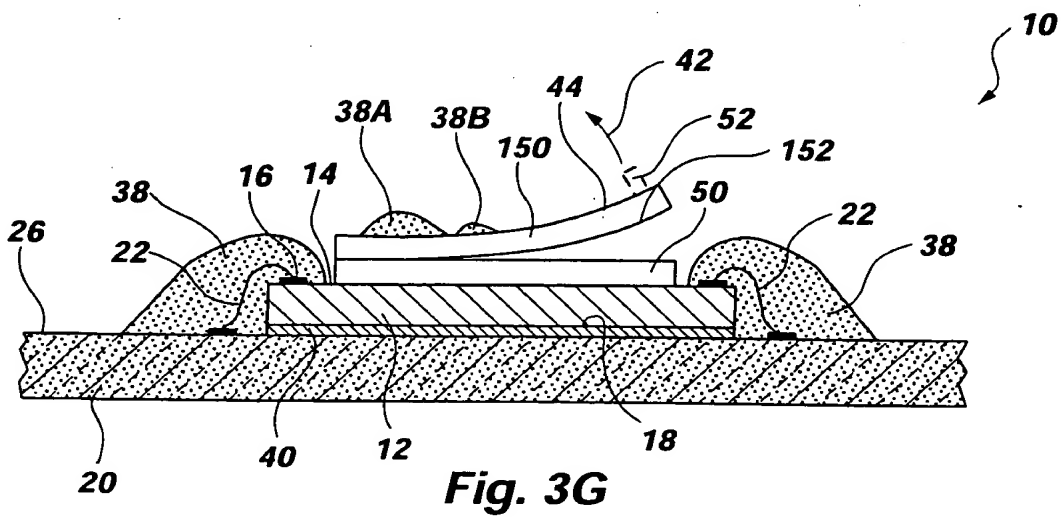

Fig. 3G

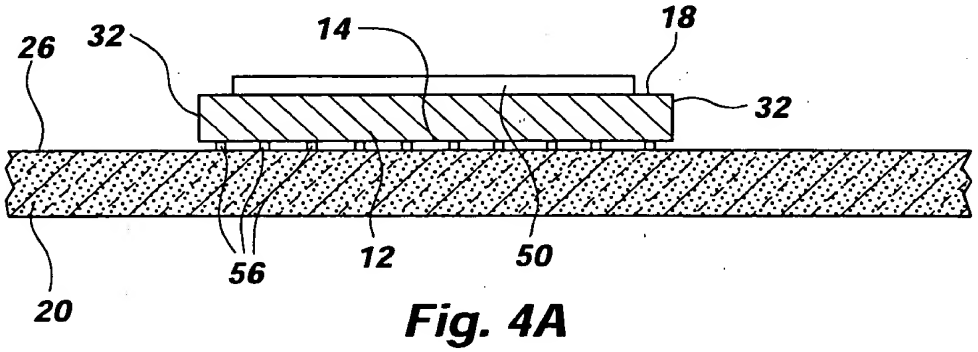

Fig. 4A

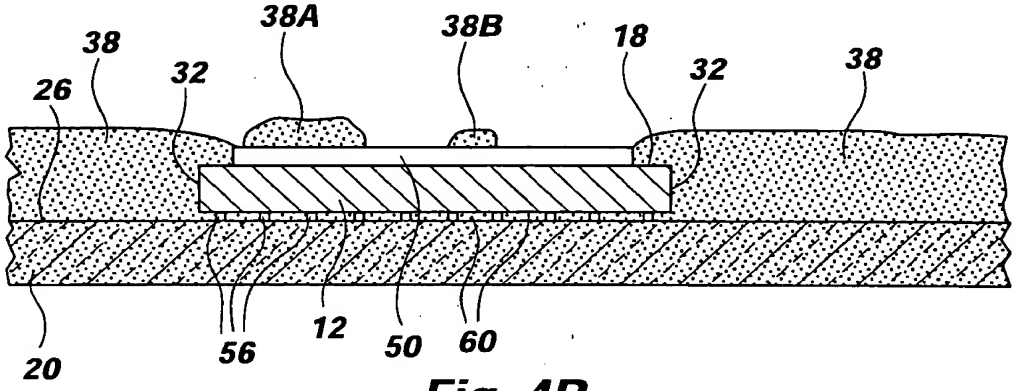

Fig. 4B

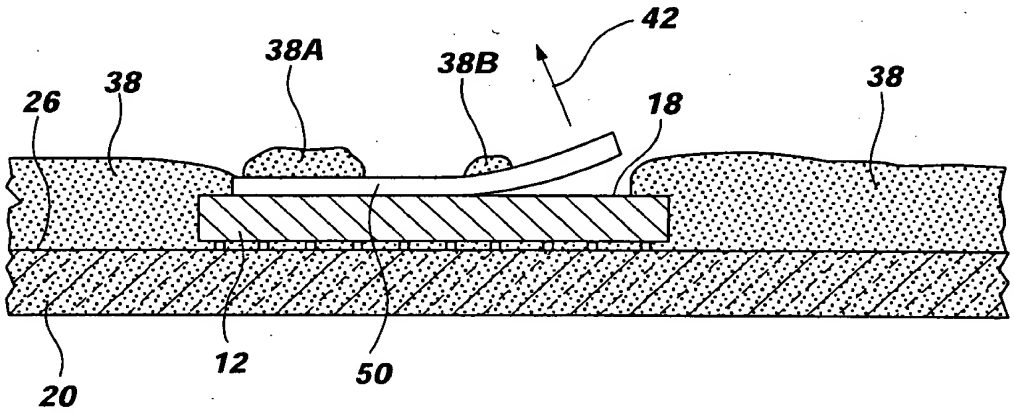

Fig. 4C

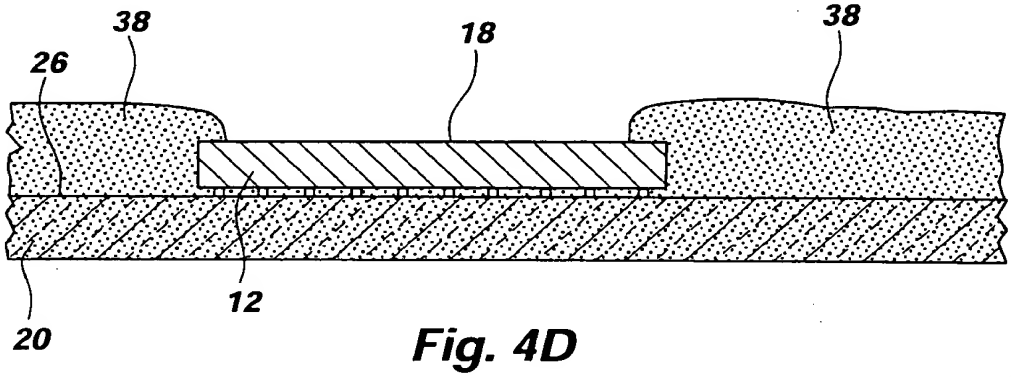

Fig. 4D

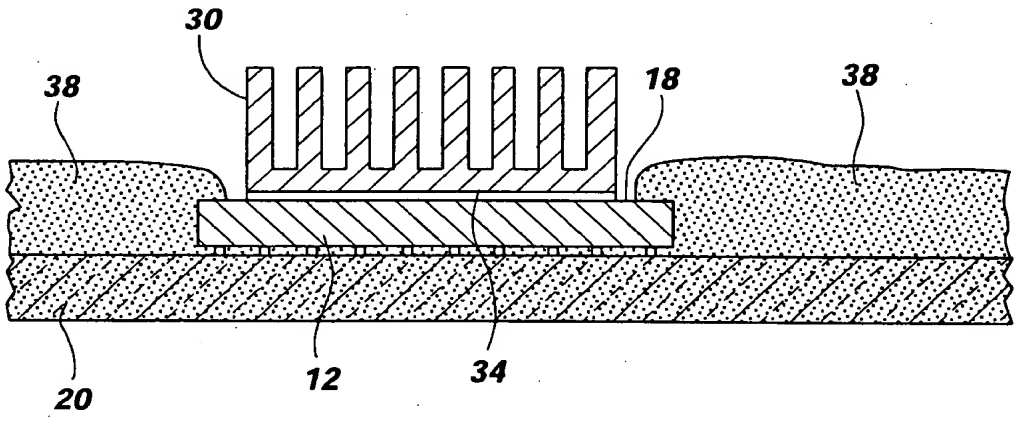

Fig. 4E

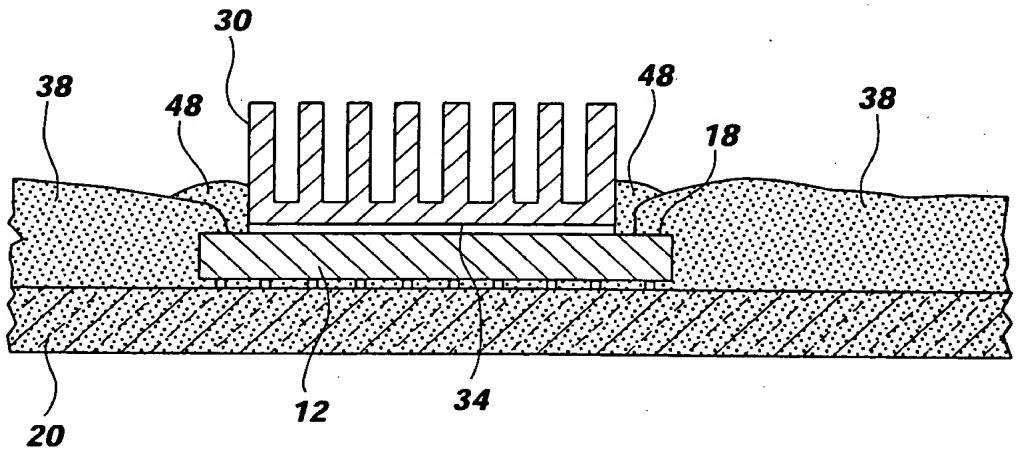

Fig. 4F